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Nanosecond Thermal Processing for Self-Aligned Silicon-on-Insulator Technology

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Advanced Technology

Nanosecond Thermal Processing for Self-Aligned Silicon-on-Insulator Technology

Ayax D. Ramirez, Bruce W. Offord, Jeremy D. Popp, Stephen D. Russell, Jason F. Rowland

Space and Naval Warfare Systems Center San Diego, CA

American Physical Society
22–26 March 2004, Montreal, Quebec, Canada

Abstract

Future radar and communications systems will have the need to use CMOS integrated circuits to provide increased analog and digital functions. Conventional CMOS technology has been locked into designing processes around polysilicon gate material because of the need for self-alignment. Low-resistance metal gates are superior for high-speed devices. However, their low melting point prevented their use in a self-aligned structure that experiences high-temperature processing (>700 ^{o}C). Silicon-on-Insulator (SOI) technology, non-refractory metal gates, and nanosecond laser processing were used to fabricate a self-aligned structure.

These techniques will allow further scaling of CMOS devices and enable mixed-mode devices to be integrated on the same substrate. The laser is used to rapidly, on the order of nanoseconds, melt and redistribute the implanted dopants for the source and drain with minimal lateral diffusion, which lowers parasitic gate to drain and source overlap capacitance. Gate resistance can be lowered by at least an order of magnitude and optimal threshold control of pMOS and nMOS devices can be achieved by using an aluminum metal gate instead of a polysilicon gate. This process allows high-performance, low-power digital technology to be integrated with high F_{max}, low-noise RF devices.

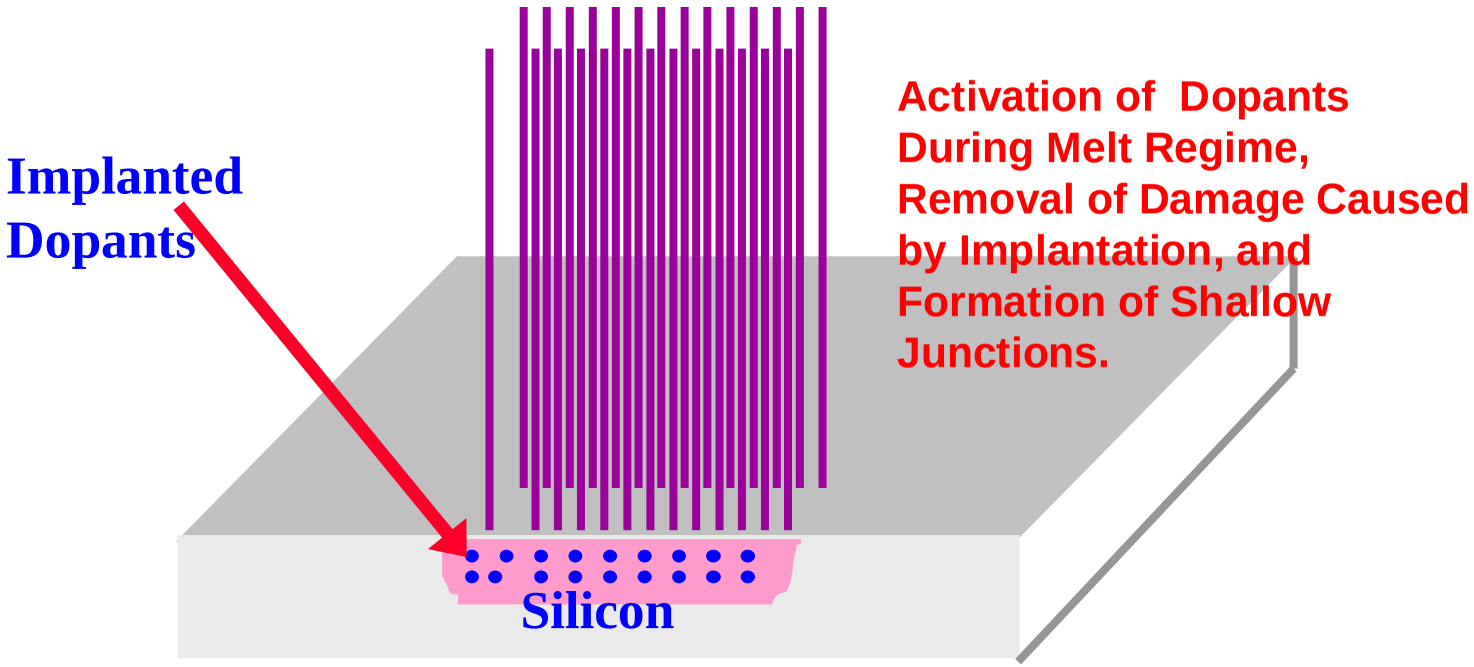
Background

There is a need for deeply scaled CMOS integrated circuits (ICs) to provide mixed-mode operation (analog and digital). As IC device dimensions decrease into the deep-submicron range, tighter control on dopant redistribution during the IC process has become more relevant. Minor variations in the dopant distribution could lead to large differences in the electrical properties of junction devices.

The need for self-alignment has dictated the use of polysilicon gates when designing CMOS devices. Because the CMOS process requires a high-temperature process to anneal the source and drain implants after the gate definition (which leads to self-alignment), metal gates were discarded. In general, low-resistivity metal gates are superior for high-speed devices as well as high Fmax and low-noise properties; however, their low melting point was what led technology to use polysilicon.

Laser Annealing and Dopant Activation

λ = 308 nm XeCl Excimer Laser

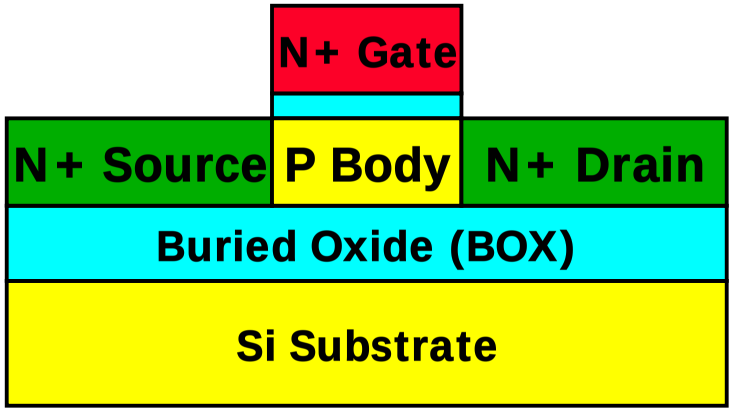


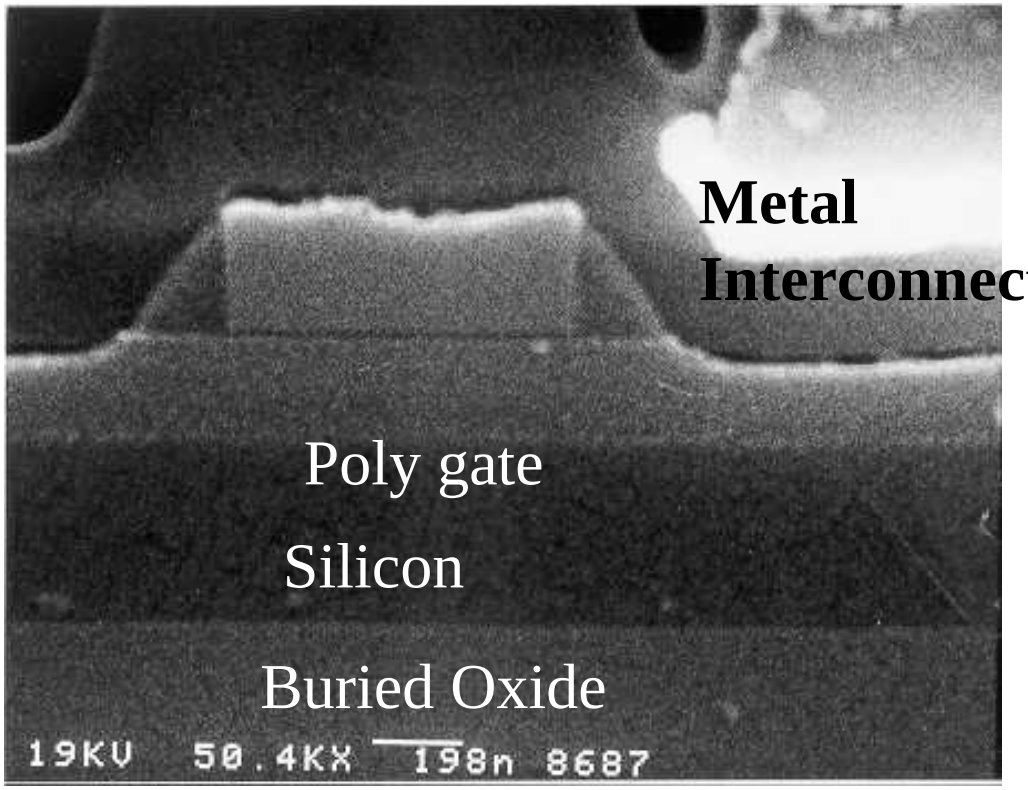
APPROACH

- Self-Aligned Metal Gate
- Silicon-on-Insulator (SOI) Technology
- Nanosecond Thermal Processing with Excimer Laser

Physical Structure of a Poly Gate (SOI) MOSFET

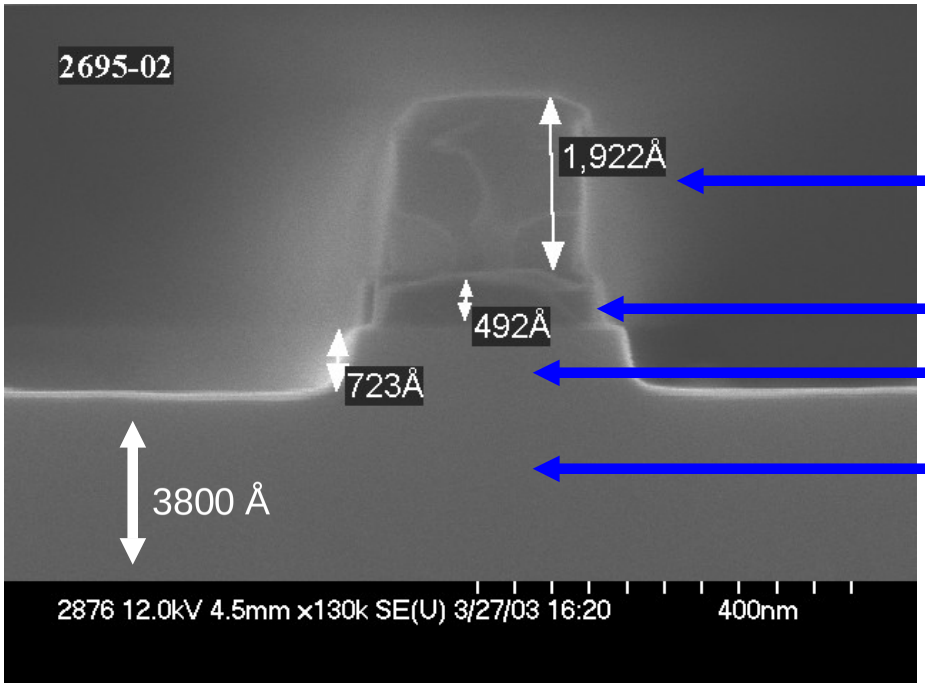
Conventional Poly Gate Technology

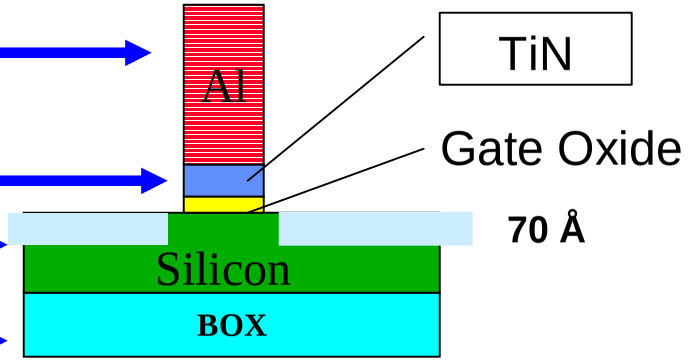




Physical Structure of a Metal Gate (SOI) MOSFET

Metal Gate Technology



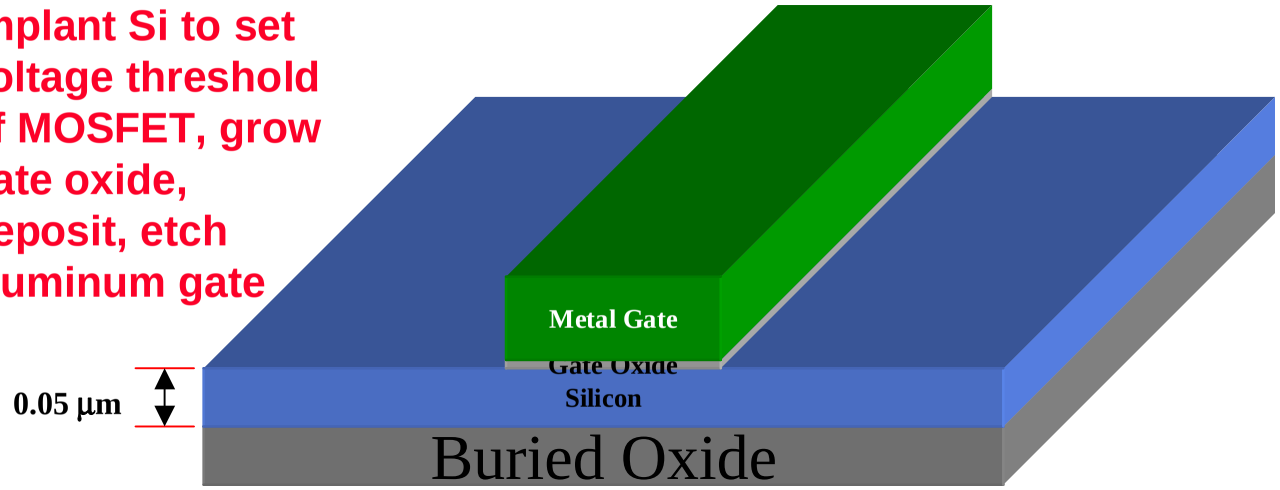


0.25-micron Gate Length

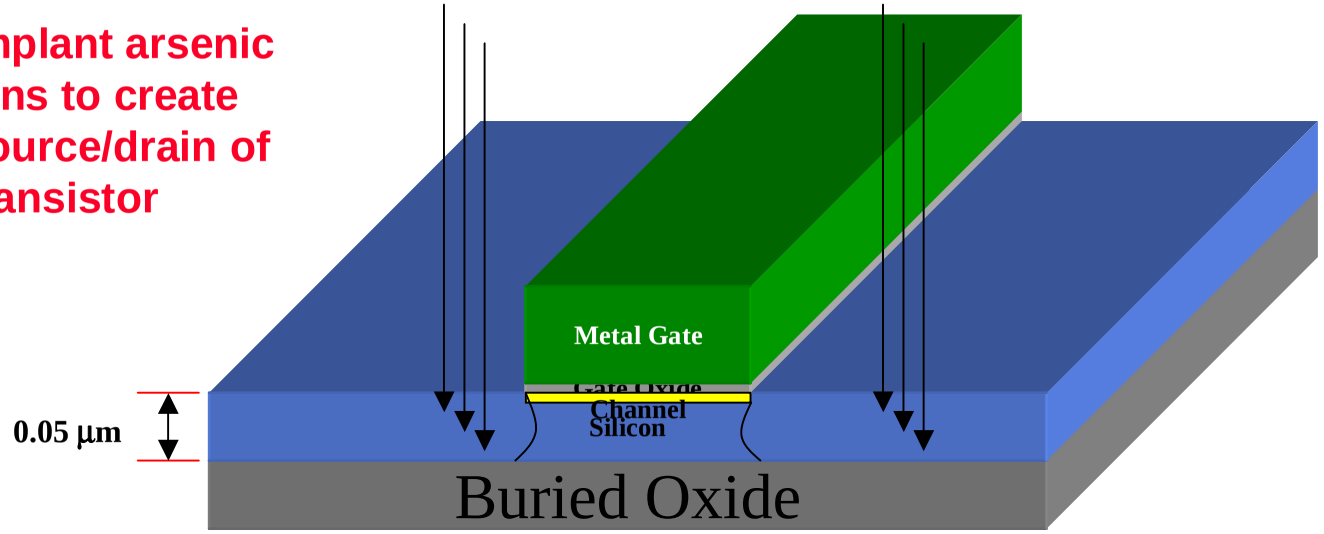
Using Al as the material for the metal gate creates a device that has at least an order of magnitude lower gate resistance than a silicide polygate.

METAL GATE (SOI) MOSFET: THE PROCESS

Implant Si to set voltage threshold of MOSFET, grow gate oxide, deposit, etch aluminum gate



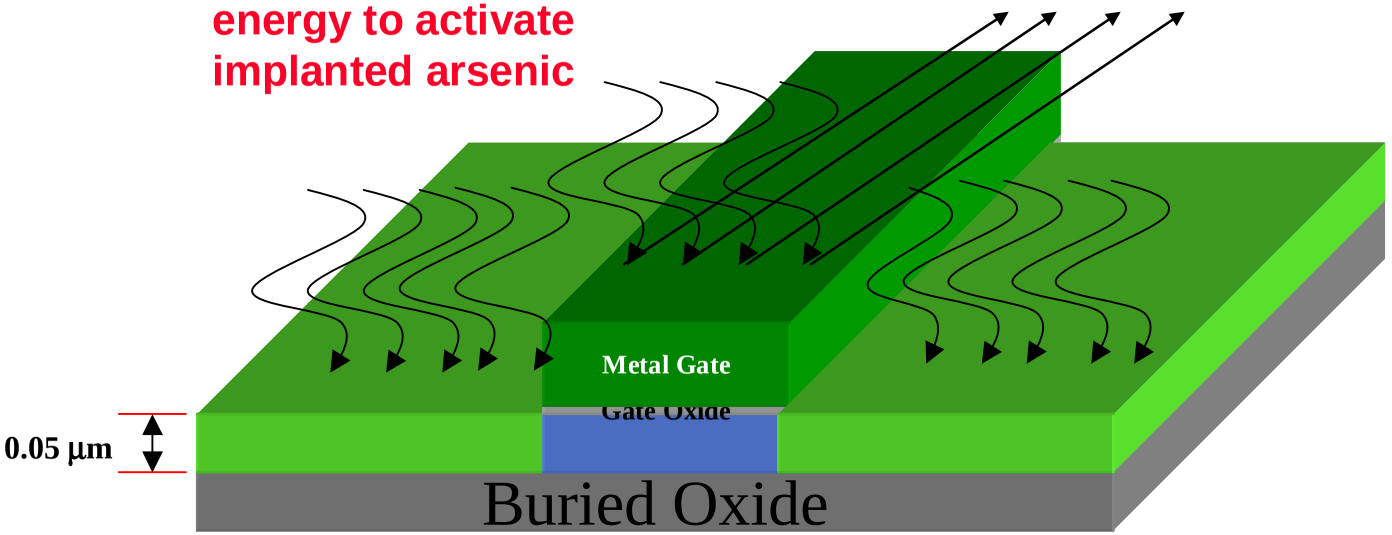
Implant arsenic ions to create source/drain of transistor



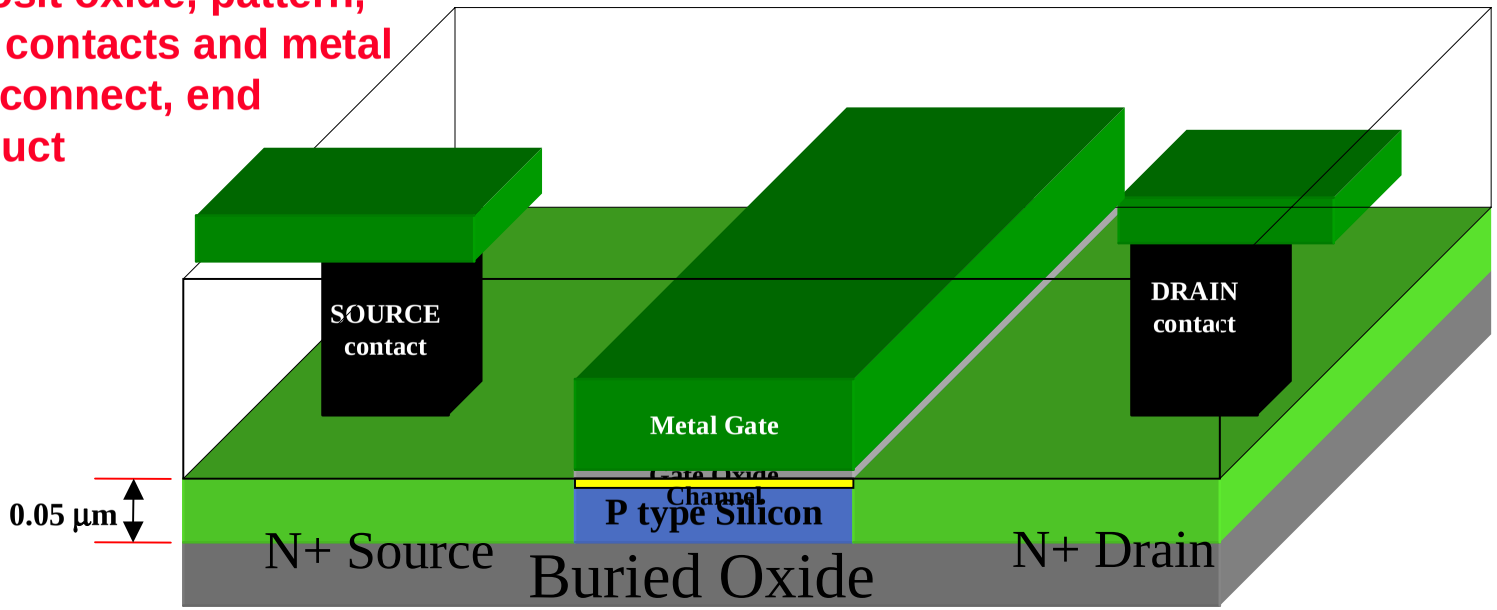
METAL GATE (SOI) MOSFET: THE PROCESS

Expose wafer to Laser energy to activate implanted arsenic

Laser Light Reflected by Metal Gate



Deposit oxide, pattern, etch contacts and metal interconnect, end product



Experimental Results

	SOI Wafers Characteristics	
Material	6-in SOI Wafer	Ion Implanted with As at a dose of $5 \times 10^{15}/cm^2$ @30 KeV
Orientation	<001>	SIMS Analysis Performed to determine carrier concentration
Si Thickness	700 Å	SRP Analysis performed to determine percent activation
SiO_2 Thickness	On a 3800Å-layer of SiO_2	
Laser	Excimer, 308 nm	
Pulse Energies	Up to 425 mJ	
Fluence	Ranged from 300 to 400 mJ/cm^2	
Pulse Rep. Rate	1 Hz	
Pressure	300 mtorr (processing chamber)	

Excimer Laser

Optics & Processing Chamber

FIG. 1 Primary Components of the Excimer Laser Processing System

Laser Annealing and Dopant Activation: SIMS Results

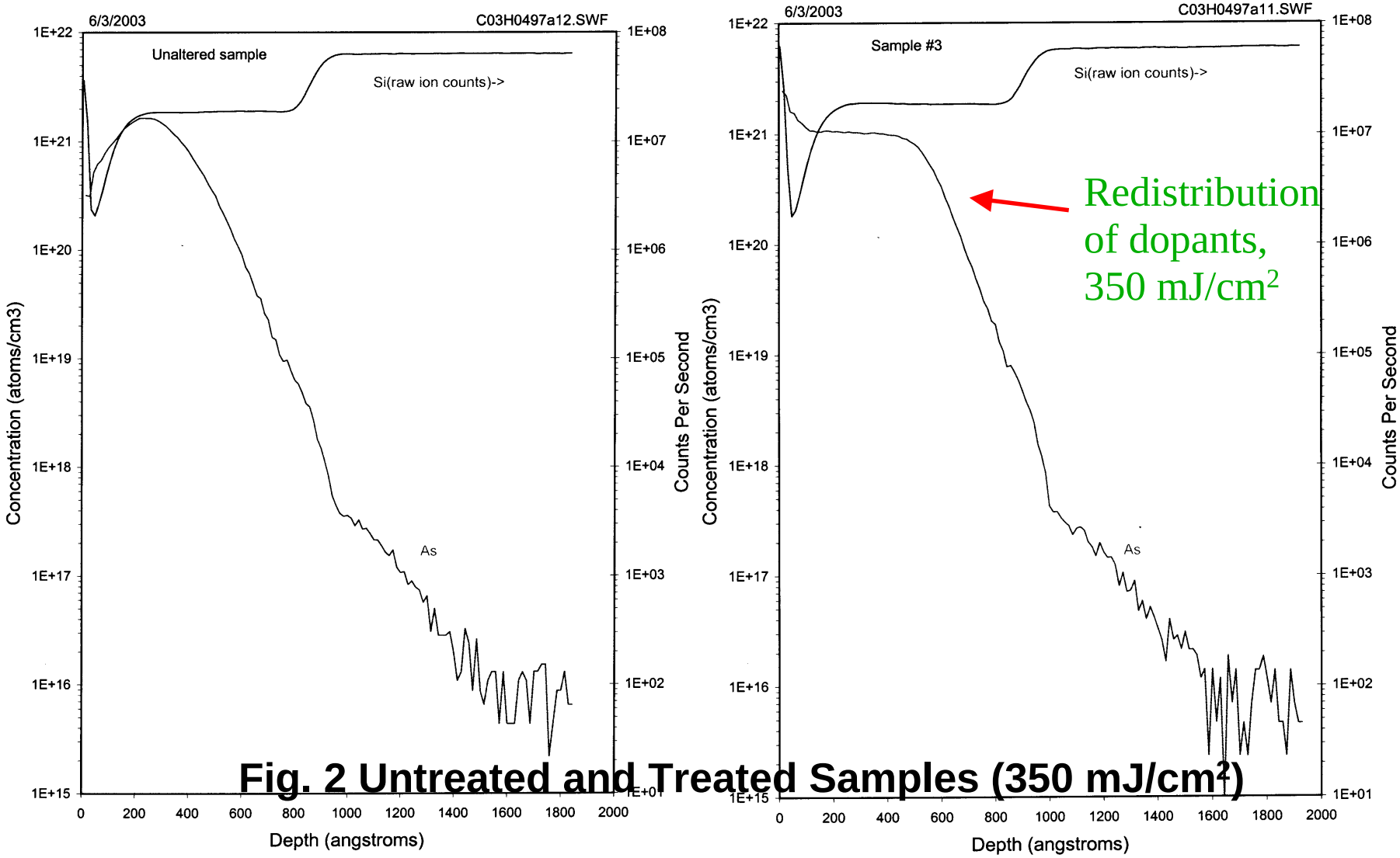


Fig. 2 Untreated and Treated Samples (350 mJ/cm²)

Laser Annealing and Dopant Activation: SRP Results

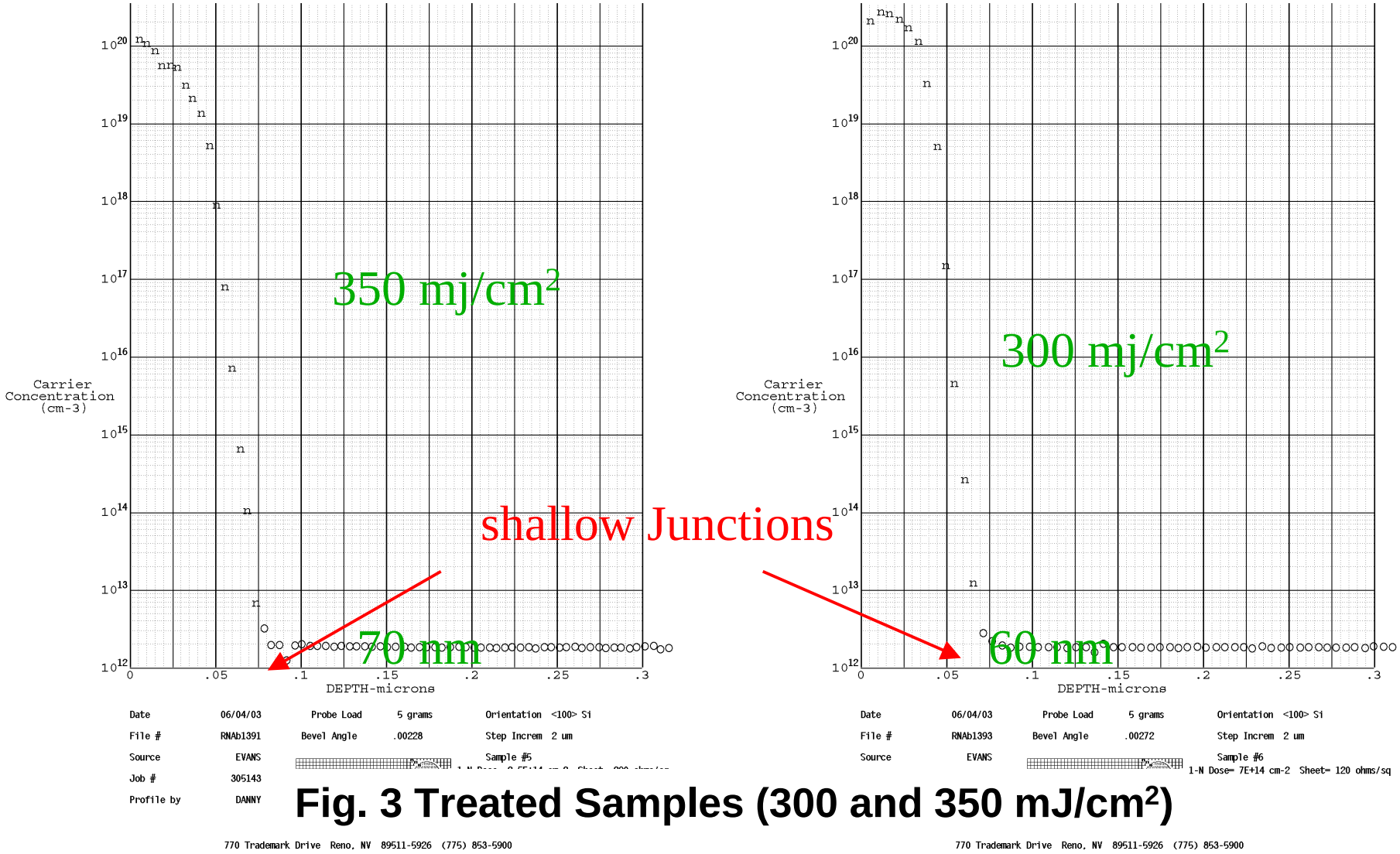


Fig. 3 Treated Samples (300 and 350 mJ/cm²)

RBS Analysis

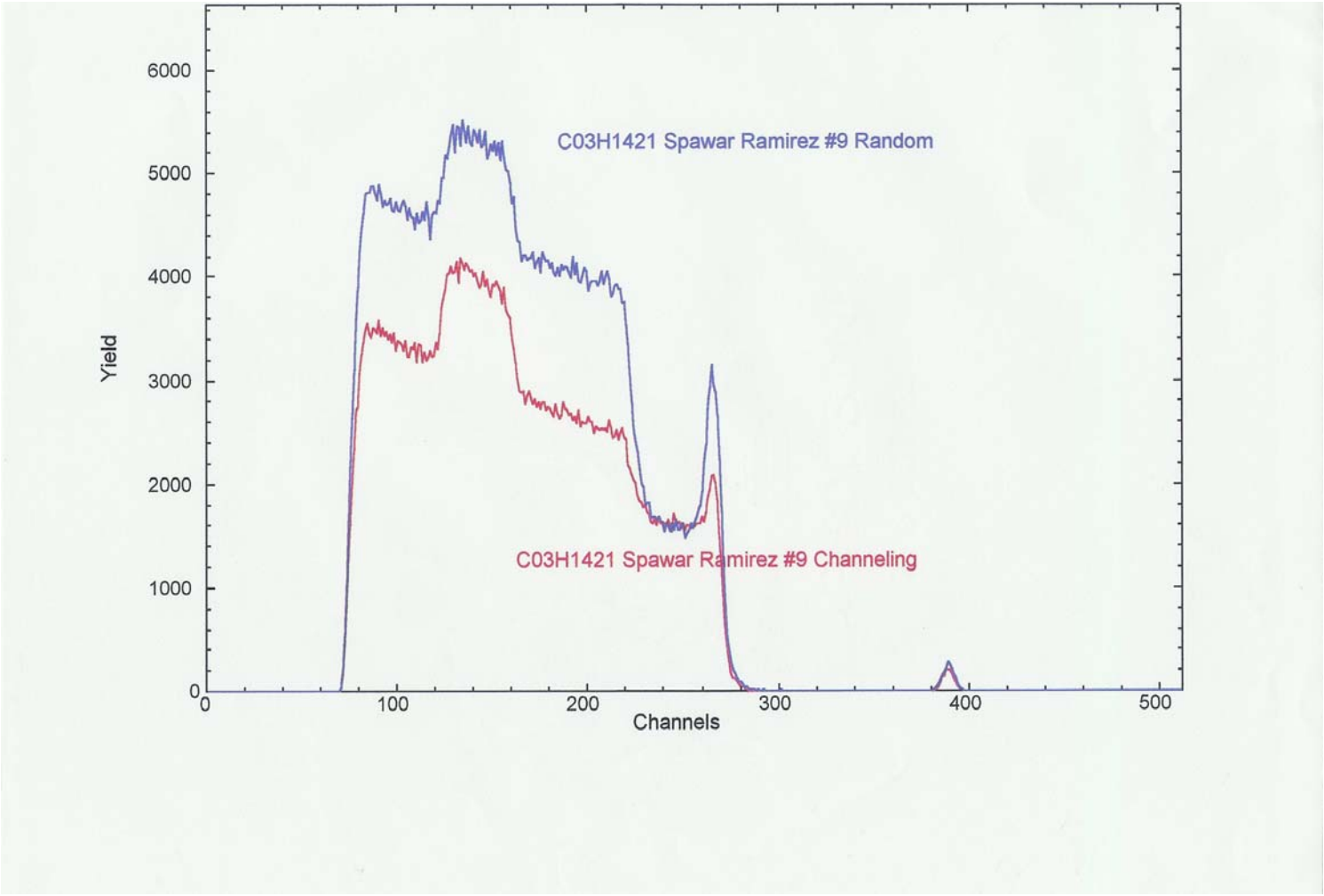


Fig. 5 Rutherford Backscattering Spectrometry (RBS) Analysis of Laser-Treated Sample

EFFECTS OF LASER UV LIGHT ON METAL LINES

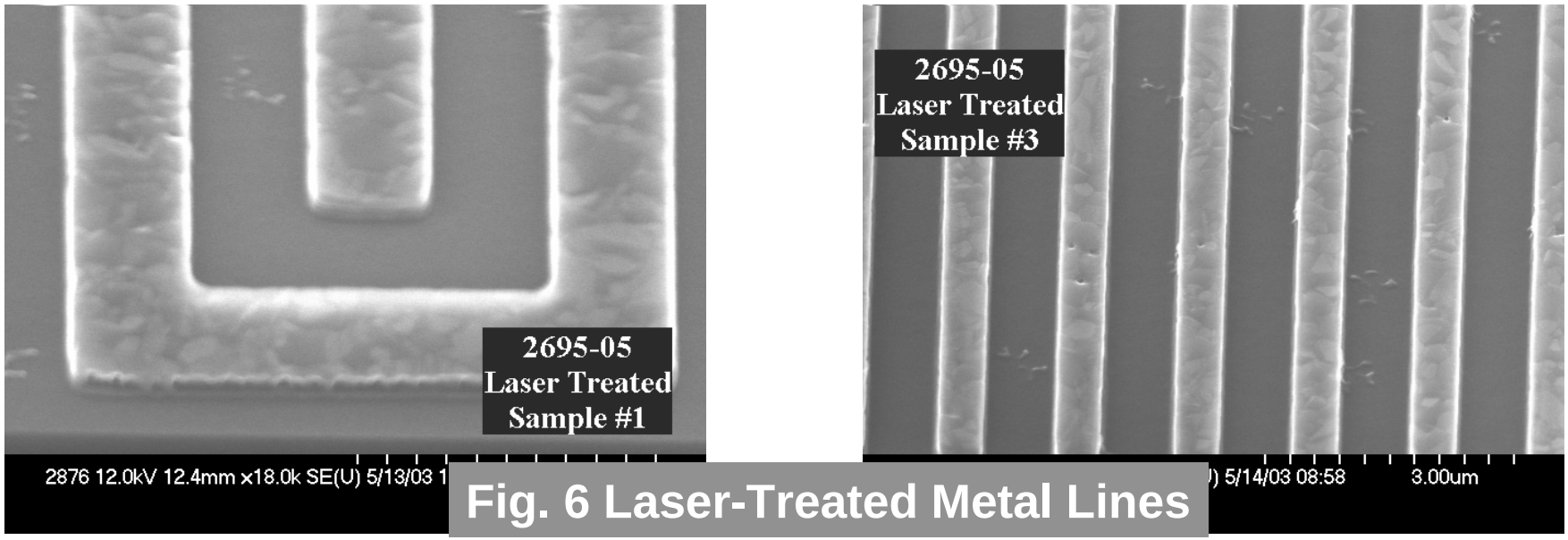


Fig. 6 Laser-Treated Metal Lines

Laser experiments were conducted to determine the effects of ultraviolet (UV) light on the metal lines. Figure 6 shows two Scanning Electron Microscopy (SEM) pictures of metal samples after exposure to five pulses (at repetition rate of 1 Hz) with fluences of up to 500 mJ/cm^2. No damage to metal lines was observed.

FIGURES OF MERIT TO QUANTIFY THE RF PERFORMANCE

Unity Current Gain Frequency

$$f_t = \frac{g_m}{2\pi\left(C_{gs} + C_{gd} + C_{gb}\right)}$$

Speed
Decrease C'$_s$ → Increase f_t

Unity Power Gain Frequency

$$f_{max} = \frac{f_t}{2\sqrt{2\pi f_t R_g C_{gd} + g_{ds}\left[R_g + R_s\right]}}$$

RF Gain
Decrease R_g → Increase f_{max}

Minimum Noise

$$F_{min} = 1 + k\frac{f}{f_t}\sqrt{g_m\left[R_s + R_g\right]}$$

Microwave Noise
Decrease R_g → Decrease F_{min}

Modeling of Gate Resistance and Source Resistance Effects on F_t/F_{max}

Assume, $w/l = 25\mu m / 0.25\mu m$, $l_{ov} = 0.1\mu m$, $C_{ox} = 4.6\ {}^{fF}/_{um^2}$, $\mu_n C_{ox} = 120\ {}^{\mu A}/_{V^2}$, $\Delta V = 1v$, $gm = 12mS$, $gds = 100\mu S$

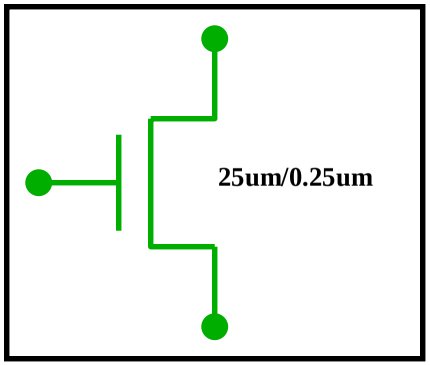
$R_{source} = R_{spacer} + R_{s,(\text{silicided or unsilicided})}$

Sheet resistances, $R_{spacer} = \dfrac{0.001\Omega cm}{0.05\mu m} 10^4\ {}^{cm}/_{um} = 200\ {}^{\Omega}/_{sq}$, $R_{si/poly,silicided} = 3\ {}^{\Omega}/_{sq}$, $R_{s,unsilicided} = 200\ {}^{\Omega}/_{sq}$, $R_{gate,sh} = 0.1\ {}^{\Omega}/_{sq}$

Worst case $R_{source} = \left(200\ {}^{\Omega}/_{sq}\right)\dfrac{0.25\mu m}{25\mu m} + \left(200\ {}^{\Omega}/_{sq}\right)\dfrac{1\mu m}{25\mu m} = 10\Omega \le \dfrac{1}{\text{gm}} = 81\Omega$

Comparison PolyGate to MetalGate (5 fingers x 5um x 0.25um),

$R_{gate,metal} = \left(0.1\ {}^{\Omega}/_{sq}\right)\dfrac{25\mu m}{(3)(5)(0.25\mu m)} = 0.67\Omega$, $R_{gate,poly} = \left(3\ {}^{\Omega}/_{sq}\right)\dfrac{25\mu m}{(3)(5)(0.25\mu m)} = 20\Omega$



$$f_{t,poly/metal} \approx \frac{gm_{eff}}{2\pi\left(C_{gs} + C_{gd}\right)} = \frac{10.7mS}{2\pi(28.75\,fF + 11.5\,fF)} = 42.3GHz$$

$$f_{\max,metal} \approx \frac{f_t}{2\sqrt{g_{ds}(R_g + R_s) + 2\pi f_t R_g C_{gd}}} = \frac{42.3GHz}{2\sqrt{100\mu S(0.67\Omega + 10\Omega) + 2\pi(42GHz)(0.67\Omega)(11.5\,fF)}} = 379.8GHz$$

$$f_{\max,poly} = \frac{42.3GHz}{2\sqrt{100\mu S(20\Omega + 10\Omega) + 2\pi(42GHz)(20\Omega)(11.5\,fF)}} = 83.8GHz$$

$$f_{\max,metal} = 4.5\, f_{\max,poly}$$

QUANTIFICATION OF THE METAL GATE PROCESS

nMOS RESULTS: IV-Curves

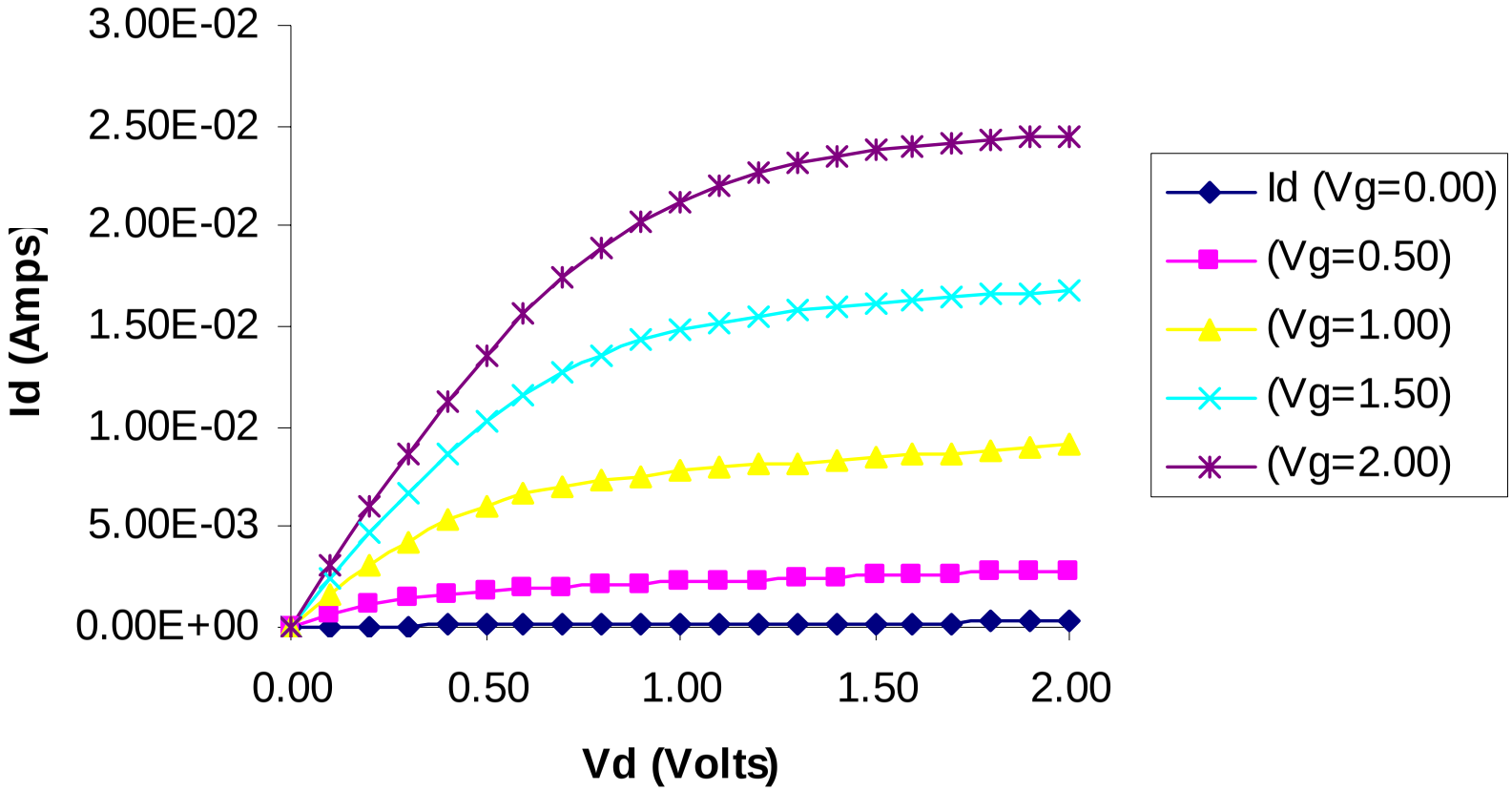


Fig. 7 Id vs. Vd for (L = 0.25, W = 70) nMOS Device

nMOS RESULTS: F_t and F_{max}

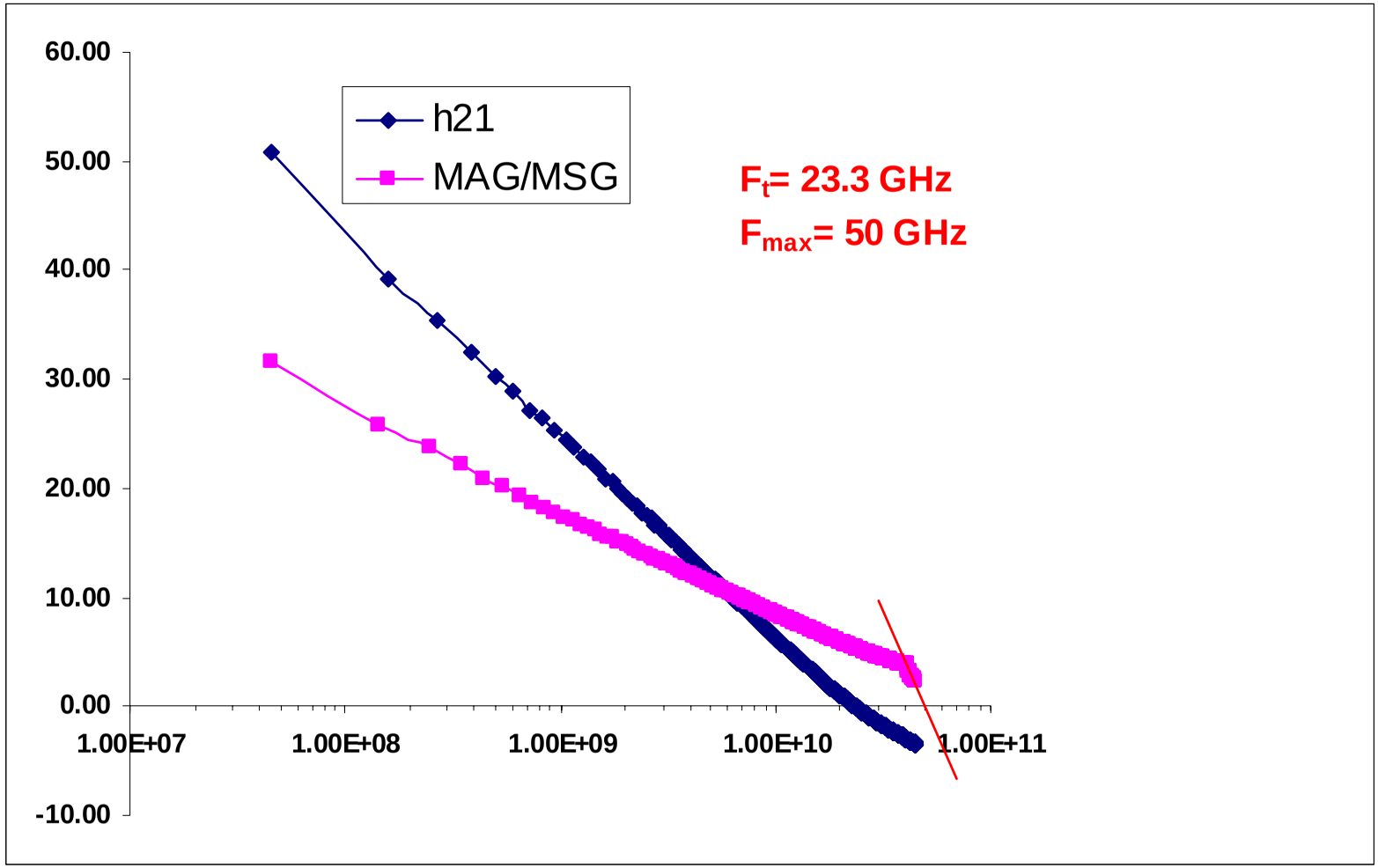


Fig. 8 F_t and F_{max} for (L = 0.25, W = 70) nMOS Device

nMOS RESULTS

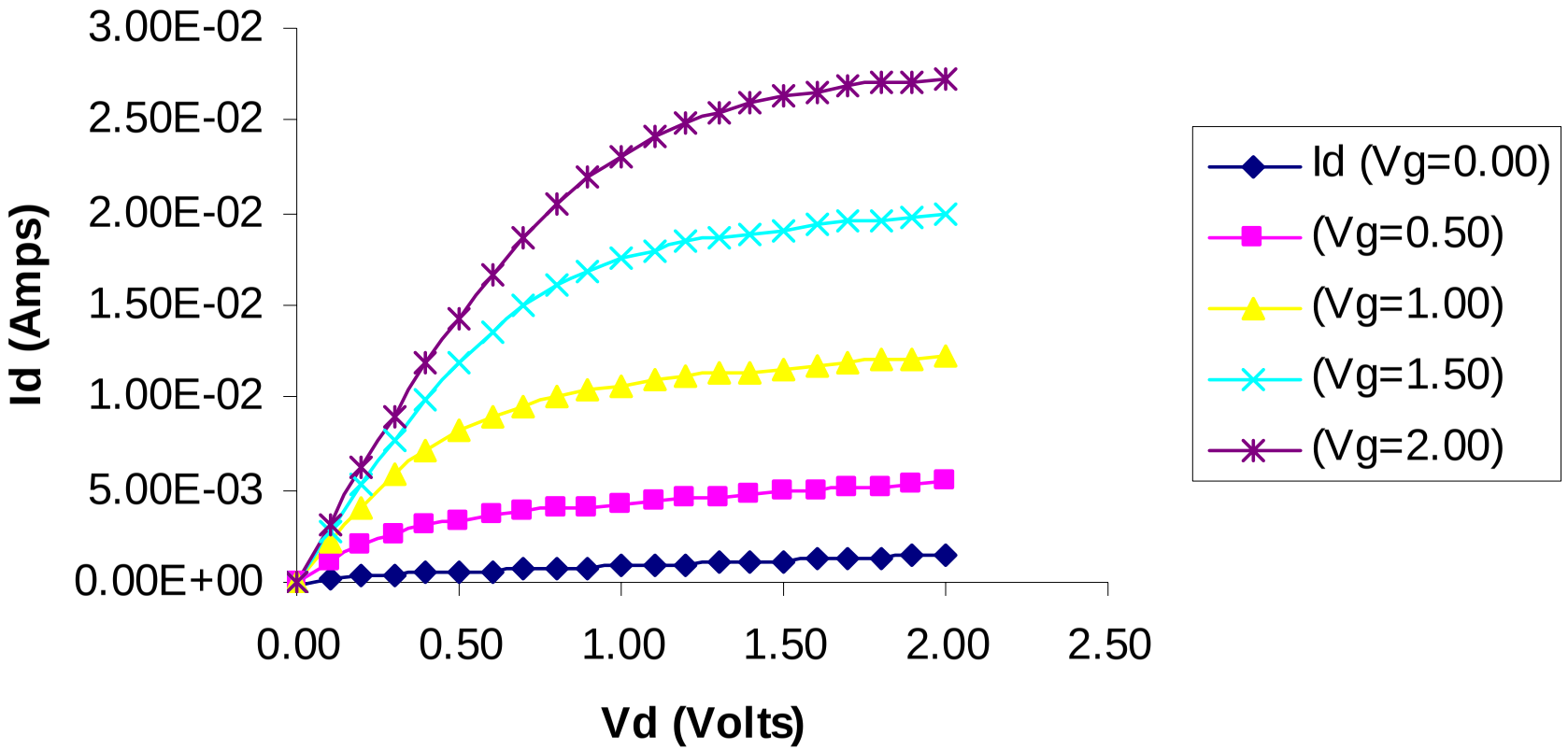


Fig. 9 Id vs. Vd for nMOS Device

nMOS RESULTS:F_t and F_{max}

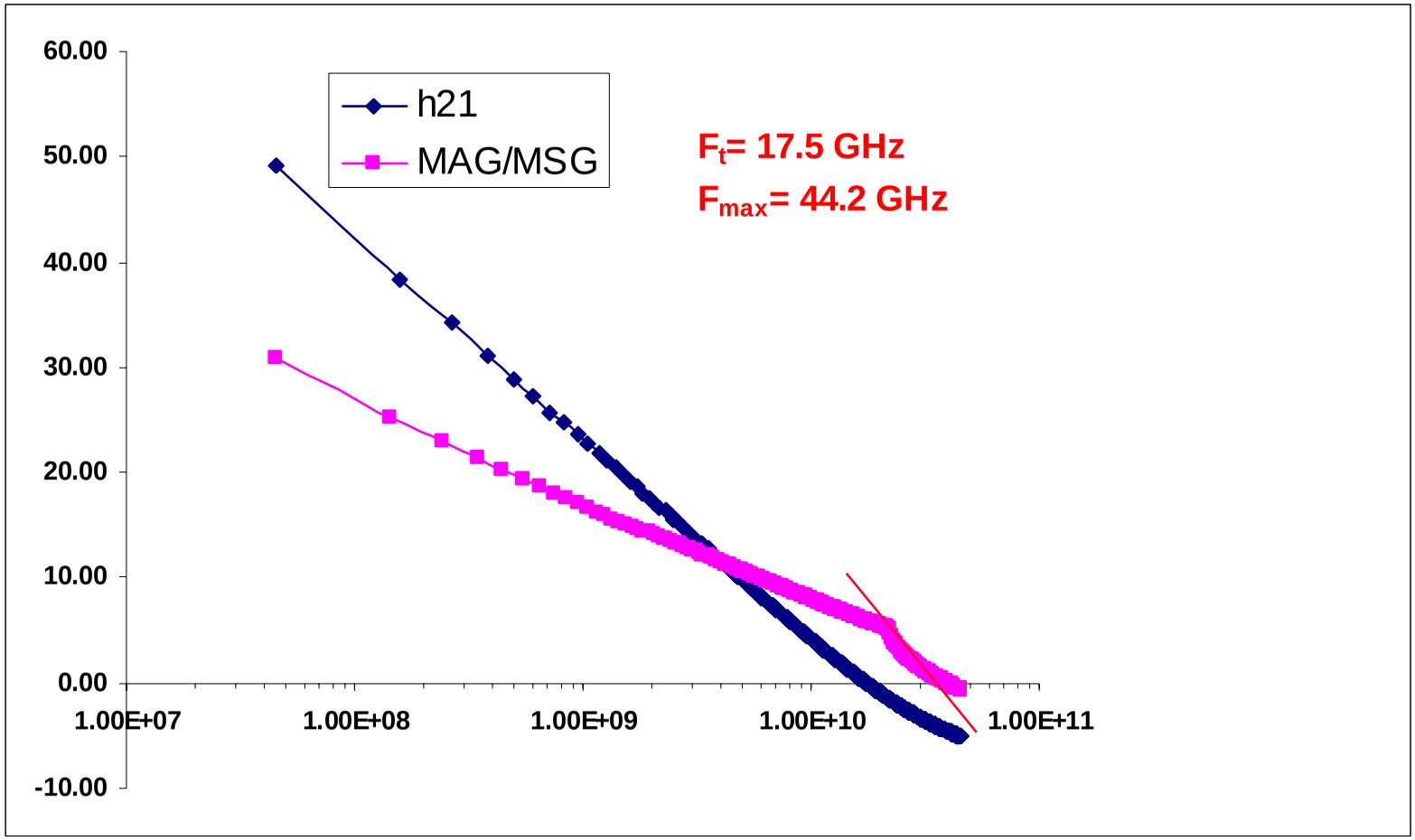


Fig. 10 F_t and F_{max} for (L = 0.25, W = 56) nMOS Device

Conclusions

1. Designed nMOS SOI devices with aluminum gate.
2. Characterized dopant profile and activation levels using Secondary Ion Mass Spectrometry (SIMS) and spreading Resistance Profiling (SRP), respectively, which demonstrated high levels of dopant activation using laser annealing.
3. Demonstrated the creation of very shallow junctions, in the order of 60 nm, using laser annealing.
4. Created nMOS devices with Id values of over 25 mA, F_t values of over 20 GHz, and F_{max} values of 50 GHz.
5. Demonstrated feasibility of SOI Metal Gate Technology using laser annealing.

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14. ABSTRACT

Future radar and communications systems will have the need to use CMOS integrated circuits to provide increased analog and digital functions. Conventional CMOS technology has been locked into designing processes around polysilicon gate material because of the need for self-alignment. Low-resistance metal gates are superior for high-speed devices; however, their low melting point prevented their use in a self-aligned structure that experiences high-temperature processing (>700 ^{o}C). Silicon-on-Insulator (SOI) technology, non-refractory metal gates, and nanosecond laser processing were used to fabricate a self-aligned structure.

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15. SUBJECT TERMS

Mission Area: Microelectronics

thermal processing	excimer laser	dopant activation	n-channel Metal Oxide Semiconductor
silicon-on-insulator	laser annealing	field-effect transistor	

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